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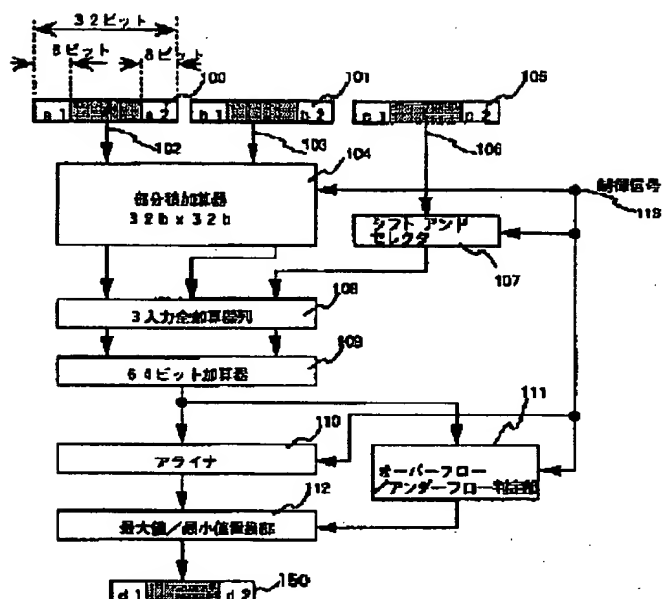
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APPLICANT : HITACHI LTD;

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TITLE : COMPUTING ELEMENT AND MICROPROCESSOR



ABSTRACT : PURPOSE: To plural product sum operations at the same times by segmenting data on a total value into values as the multiplication results of respective multiplicands of a 1st register and multipliers of a 2nd register corresponding to them, and finding multiplication results corresponding to pairs of the multiplicands and multipliers as to the respective pairs.

CONSTITUTION: The data on the total sum $N+M$ are used and the two multiplicands a_1 and a_2 packed in the 1st register 100 and the two multipliers b_1 and b_2 packed in the 2nd register 101 are inputted to a partial sum adder 104. Then multiplication $a_1 \times b_1$ and multiplication $a_2 \times b_2$ are separately performed. Two addends c_1 and c_2 packed in a register 105 are inputted and their figures are matched by a shift and selector 107. The two outputs of the partial product adder 104 and the output of the shift and selector 107 are added together and a three-input full-adder array 108/64-bit adder 109 can perform product sum operations while $a_1 \times b_1 + c_1$ and $a_2 \times b_2 + c_1$ are separated.

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